A Compact 16 Watt X-Band GaN-MMIC Power Amplifier

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***Abstract* — GaN MMIC power amplifiers for X-Band applications are presented delivering more than 16 W of cw output power while being extremely small in chip size. With a single-device amplifier on a 1.8x2.2 mm^2 chip 7.8 W output power at 8 GHz are achieved with a maximum PAE of 44%. On a chip of 2.2x3.3 mm^2 size only, a two-stage amplifier is realized with 18 dB of linear gain and 16 W cw output power at 8 GHz. PAE of the MMIC reaches 30%.**

***Index Terms* — Gallium Nitride, MMIC Power Amplifier, X-Band, Coplanar Wave Guide (CPW)**

I. Introduction

Due to its promising physical properties, GaN has received a rapidly growing interest in the research community over the last years and presently is considered to be the semiconductor material of choice for high power microwave applications. Key feature is that GaN-HEMTs allow high-voltage operation without sacrificing speed. This is of particular interest also for power amplifiers in X-Band, e.g. for satellite transmitters or radar applications.

While high power densities of single and often small devices have been reported in the literature (e.g., [1] [2]), there are only a few publications on high absolute output power or the development of fully integrated MMICs in the X-Band range [3] [4] [5]. The latter case, i.e., the monolithic realization of an amplifier module, is very advantageous in this frequency range because the packaging parasitics of discrete transistors become severe, thus limiting the potential of hybrid modules. The MMICs published in [3] [4] [5] deliver saturated output powers of 8 W cw [3], 13.4 W pulsed [4] for GaN on SiC and 25 W pulsed [5] for GaN on Si.

Besides the power performance, however, also chip size needs to be considered for a GaN MMIC, the more because the material (particularly GaN on SiC) is extremely expensive. To this end, the MMICs published so far are relatively large, occupying 4.1x6.3 mm^2 [3] or 3x4.5 mm^2 [4] [5]. Thus, shrinking the chip dimensions is a necessity when aiming at practical applications.

This is the issue addressed in this paper. It is shown that competitive power performance (16 W cw) can be achieved at half the chip size of previous work [3,4,5]. To our knowledge, the presented amplifiers are the smallest of their kind delivering more than 10 W of continuous-wave output power in X-Band.

The paper is organized as follows: Sec. II provides details on device technology and the properties of the AlGaN/GaN-HEMT transistor cell, Sec. III explains the circuit design issues. The probably most important part is Sec. IV, where the measurements results are presented and discussed. Different amplifier versions were designed and processed in order to obtain a more systematic understanding. The paper ends with the conclusions in Sec. V.

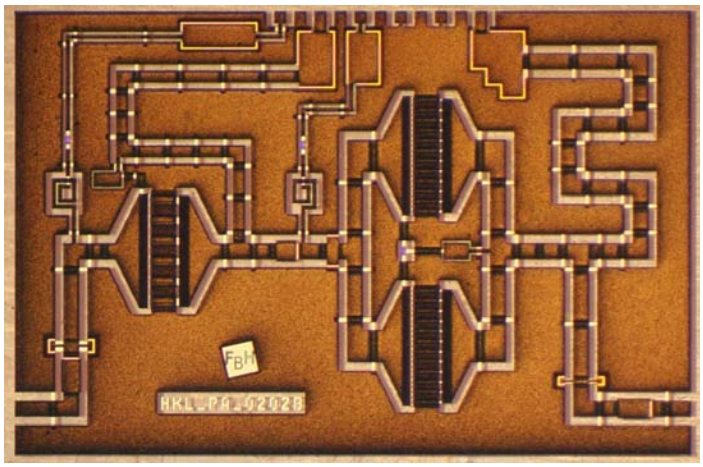

Fig. 1. Chip photo of the two stage power amplifier PA0202B. Chip size is 2.2 x 3.3 mm^2, transistor size: 12x125 µm (driver stage) 24x125 µm (power stage).

II. Device technology

The HEMT epitaxial structure was grown by MOVPE on a 2" s.i. SiC substrate at the Fraunhofer institute IAF, Freiburg, Germany. The structure consists of a 2.3 µm GaN buffer layer, an undoped 25 nm $Al_{0.3}Ga_{0.7}N$ barrier layer and a 2 nm GaN cap layer. An averaged sheet resistance of 420 Ω/sqr was measured using Van-der-Pauw structures on the passivated wafer.

The MMIC process starts with the fabrication of the ohmic contacts using a metalization consisting of evaporated Ti/Al/Ti/Au and a sputtered WSiN cap layer. Annealing of the ohmic contacts at 830°C results in a contact resistance of 0.6 Ωmm. The mesa structures are defined by reactive ion etching applying an $Ar/BCl_3/Cl_2$ plasma. We apply 2" stepper technology for all steps except for defining the 0.4 µm T-shaped Pt/Au gates where electron-beam lithography is used. Si_3N_4 MIM capacitors and NiCr resistors complete the coplanar MMIC process. The MIM capacitors are adapted for high-voltage circuits.

Regarding the transistor cell, 2x50 µm devices demonstrate an averaged maximum transconductance of $g_m = 235$ mS/mm and an averaged saturation current of $I_{DSS} = 1.2$ A/mm at

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TABLE I
PERFORMANCE SUMMARY OF THE 1-STAGE AND 2-STAGE AMPLIFIERS

		Large Signal Performance (8GHz)				
Circuit	Chip size mm^2	Drain Bias (V)	Linear Gain (dB)	P-1dB (W)	P-3dB (W)	Max PAE (%)
DA0101A	1.8x2.2	20	10.7	6.1	7.8	44
PA0202B	2.2x3.3	28	18.2	13.4	16.1	30

V_{GS} = +2 V. They exhibit a cutoff frequency f_T of 25 GHz and a maximum oscillation frequency of 76 GHz at the bias point V_{DS} = 20 V and V_{GS} = -4.5 V.

III. CIRCUIT DESIGN

The main goal was to demonstrate the capabilities of GaN in achieving several contrasting design targets simultaneously to an extent, which was extremely difficult or even impossible to obtain with other technologies. More precisely, we aimed at realizing an X-Band power amplifier being small in chip size with high gain (above 15 dB) and a maximum output power above 15 W. While the technology used can be operated above 30 V, the circuits were dimensioned for a drain bias voltage of 28 V.

In designing these amplifiers, we went through different steps starting with the single HEMT cell. Its optimum Γ_{LOAD} was known from load-pull measurements and used for the design of a single-cell amplifier (DA0101A) with a 12x125 µm transistor. This amplifier served as a verification of the design methodology.

In a similar way, the power stage of the two-stage amplifier PA0202B was designed using the measured optimum Γ_{LOAD}. In contrast, the interstage- and input matching is based on measured S-parameters, i.e., assuming small-signal conditions. In order to achieve high absolute output power while maintaining small chip size the transistors used for the power stage had twice the number of gate fingers and half the pitch compared to the transistor in the driver stage. This, of course, is expected to reduce the power per gate width, which is often used as a quality indicator in the literature. In the end, however, the real figure of merit is not power per gatewidth but power per transistor area or, in the MMIC case, power per circuit size. Thus varying the total gate width while keeping size constant is an interesting degree of freedom in optimizing a circuit.

As the devices show very high gain, especially at lower frequencies, feedback networks need to be integrated to maintain stability. When matching the input and output, we get $|S_{11}| > 1$ and stability factor $k < 1$ in a frequency range around 3 GHz which implies possible oscillations. A connection of drain and gate with a resistor and a capacitor in series eliminates this problem. Possible odd-mode oscillations of the two-transistor output stage which cannot be detected in simulation by using the simple k-factor method are prevented by a resistive connection of the gates. A detailed description of the odd-mode oscillation problem and its solution is described in [6].

Fig. 1 shows a chip photo of the two-stage amplifier PA0202B. Total chip size is 2.2x3.3 mm^2, i.e., 7.3 mm^2, which is about half the size of the MMICs presented in [4] and [5]. This is achieved by using only two transistors in the output stage (i.e., devices with relatively large gate periphery). Furthermore, the coplanar layout was optimized by designing the line segments as short as possible and by folding longer segments. This principle also helps in keeping line loss low.

In order to allow tuning the circuits after a wafer has been processed, the feedback networks were connected to the output lines via air bridges, which can be removed easily, thus modifying the transmission properties. In a similar way, the input and output matching networks can be adapted during on-wafer characterization. This practice is well-known from GaAs MMIC fabrication and proves to be very efficient for GaN MMICs as well.

IV. MEASUREMENT RESULTS

In this section, the measured performance of the power amplifiers is presented. All data was measured on-wafer, with the chuck cooled to keep it at room temperature independently of the dissipated power. For comparison, load-pull data of the single transistor without any bias and matching network is included in subsection A.

A. Single Transistor

Load-pull measurements of the single transistor of 12x125 µm gate periphery at V_G = -4V and V_D = 28 V show an output power of 7.8 W and 10.7 W at the P_{-1dB} and P_{-3dB} points, respectively. This corresponds to a saturated output power of 7.1 W/mm. The maximum PAE is 45% (53% at 20 V). The transistor could be operated at voltages up to 34 V, delivering P_{-1dB} = 9.5 W and P_{-3dB} = 12.4 W (i.e., 8.2 W/mm). This data forms the basis for the output powers to be expected from the MMIC amplifier. However, the lower Q values of the on-chip transformation elements and the losses in the combining networks will cause degradations.

B. Single-Stage Amplifier (DA0101A)

The measured S-parameters of the MMIC with a single transistor (DA0101A) are plotted in Fig. 2. Since the circuit is measured in 50 ohms environment, the magnitude of S_{21} directly provides the gain value in the small signal case, which

corresponds to the linear gain of the large signal measurements. It exceeds 10 dB in the frequency range from 5.5 GHz to 9.5 GHz.

Fig. 3 shows the power performance of this amplifier for a frequency of 8 GHz, about in the center of the above-mentioned frequency band. The measured output power reached P_{-1dB} = 6.1 W and P_{-3dB} = 7.8 W, with a maximum PAE of 44%. To our knowledge, this is the highest PAE achieved for a GaN MMIC power amplifier to date. With a linear gain of 11 dB (and, accordingly, 8 dB for P_{-3db}) this MMIC provides reasonable amplification, but does not offer any gain margins. Therefore, a two-stage design as described in the following subsection is highly desirable.

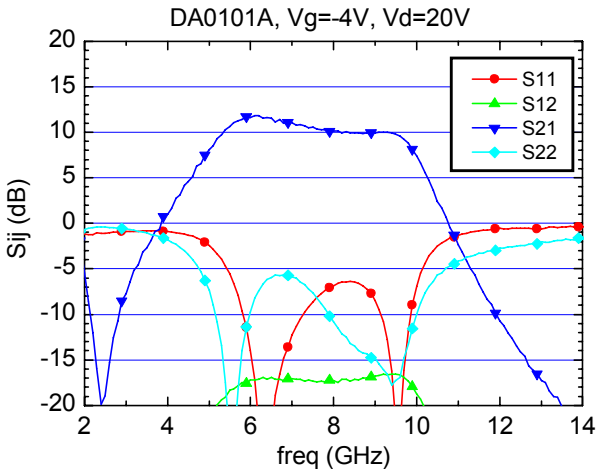

Fig. 2. Measured S parameters (magnitude) of the single-stage amplifier DA0101A against frequency at a drain bias voltage V_d of 20 V.

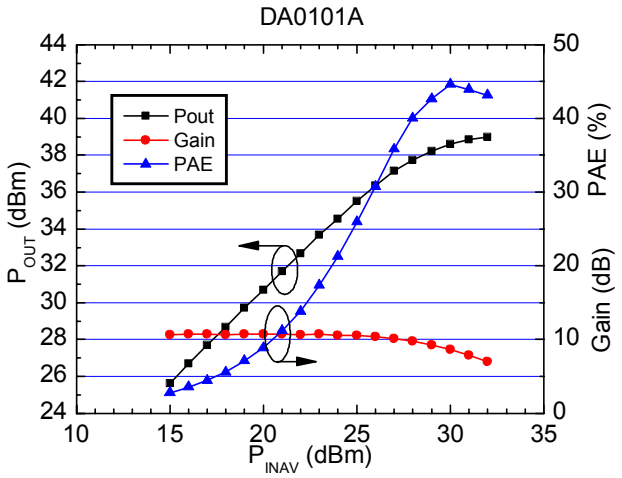

Fig. 3. Power performance (output power, gain, and PAE against input power) of the single stage amplifier DA0101A, at 8 GHz and V_D = 20 V.

B. Two-Stage Amplifier (PA0202B)

As described in Sec. III, a two-stage amplifier was developed with a two-transistor output stage. A 12x125 μm^2 HEMT in the first stage is chosen while the output stage is based on HEMTs of same periphery area, but larger gate width (24x125 μm^2).

In Fig. 4, the S-parameter characteristics of the amplifier PA0202B are plotted. A linear gain of 18 dB is obtained at 8 GHz. As can be seen from input and output return loss, a further increase in gain and bandwidth can be expected from a redesign of the matching networks.

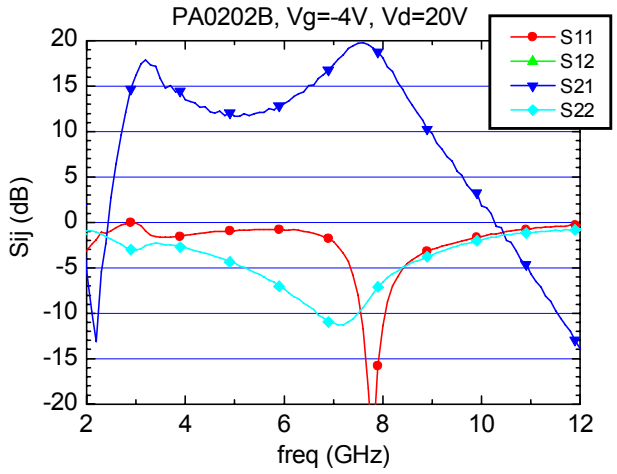

Fig. 4. Measured S parameters (magnitude) of the two-stage amplifier PA0202B against frequency at a drain bias voltage V_d = 20 V.

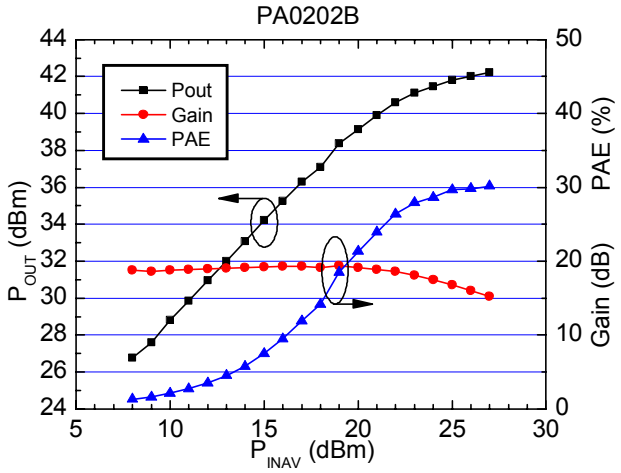

Fig. 5. Power performance of the two-stage amplifier PA0202B, at 8 GHz and V_D = 28 V.

Fig. 5 presents the power performance of the MMIC at 8 GHz. Output power, gain, and efficiency of the amplifier are plotted as a function of the available input power, which, due to the low input reflection, is approximately equal to the actual

input power and slightly underestimates gain. The results are summarized in Table I.

Output power reaches 16.1 W for the –3 dB point and 13.4 W at the –1 dB level under cw conditions. This exceeds the pulsed results of [3,4] and compares well with the pulsed 25 W power level of [5]. A maximum PAE of 30% is attained. Finally one should note that these results are obtained with a circuit of only 7.3 mm^2.

V. Conclusions

Coplanar GaN-on-SiC MMIC power amplifiers for 8 GHz have been realized focusing on compact design without sacrificing technical performance. Our two-stage version demonstrates a P_{-3db} continuous-wave output power of 16.1 W for 18 dB of linear gain and 30% PAE (drain efficiency of the output stage alone is 37%). These results are very competitive with previous work but are achieved at almost half the chip size. Since chip area is expensive for GaN-SiC-substrates, this improvement marks an important step towards making GaN MMICs for X-Band applications a reality.

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